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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,025	09/27/2004	Tadahiko Sakai	2004_1461A	3434
513 7590 02/25/2008 WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021				
EXAMINER HARRISON, MONICA D				
ART UNIT 2813		PAPER NUMBER		
MAIL DATE 02/25/2008		DELIVERY MODE PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/509,025

**Applicant(s)**

SAKAI ET AL.

**Examiner**

Monica D. Harrison

**Art Unit**

2813

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4, 6 and 9-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-20 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 9, 10, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Applicant's amendment filed 10/23/07 has been entered. Examiner acknowledges claims 21 and 22 have been added.

#### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takigawa et al (5,844,309) in view of Hotta et al (6,023,096).

2. Regarding claim 1, Takigawa et al discloses a semiconductor device comprising: a semiconductor element that has a first surface on which an external connection terminal (Figure 2, reference 26) is formed and a second surface opposite the first surface (Figure 2, reference 16); a plate that faces the second surface (Figure 2, reference 30); and a resin binder that adheres the second surface and the plate, wherein the plate has a rigidity higher than that of the semiconductor element (Figure 2, reference 42); wherein the second surface of the semiconductor element comprises a surface-finished surface such that the second surface of the semiconductor element is free from having a damaged layer thereon (Figure 2, reference 16); wherein an outer shape of the plate is larger than that of the semiconductor element (Figure 2, reference 30); and wherein the resin binder covers a peripheral side face of the semiconductor element, and furthermore at a portion that is interposed between the second surface and the plate

the resin binder allows the semiconductor element to deform in a thickness direction thereof (Figure 2, reference 42).

However, Takigawa et al does not disclose the semiconductor has a thickness of  $1\mu\text{m}$  or more and  $150\mu\text{m}$  or less.

Hotta et al discloses the semiconductor has a thickness of  $1\mu\text{m}$  or more and  $150\mu\text{m}$  or less (column 6, lines 42-46).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Takigawa et al, with the teachings of Hotta et al, for the purpose of forming a semiconductor device having metal foil integral with sealing resin.

3. Regarding claim 2, Takigawa et al discloses wherein the resin binder covers at least an edge defined by a side face and the second surface of the semiconductor element, about the outer periphery of the semiconductor element (Figure 2, reference 42).

4. Regarding claim 3, Takigawa et al discloses wherein the resin binder covers the side face over an entire circumference of the semiconductor element (Figure 2, reference 42).

5. Regarding claim 4, Takigawa et al discloses wherein the resin binder covers only a corner of the side face of the semiconductor element (Figure 2, reference 42).

6. Regarding claim 6, Takigawa et al discloses wherein the external connection terminal is provided with a bump (column 37, lines 45-50).

7. Regarding claim 9, Takigawa et al discloses wherein the semiconductor element includes a re-wiring layer on the first surface, the re-wiring layer has a surface electrode formed on a surface and an internal electrode formed inside thereof, and the internal electrode connects the surface electrode and the external connection terminal (Figure 2).

8. Regarding claim 10, Takigawa et al discloses wherein the surface electrode is provided with a bump (column 37, lines 45-50).

9. Regarding claim 22, Takigawa et al discloses wherein the first surface of the semiconductor element is exposed from the resin binder (Figure 2, reference 16).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takigawa et al (5,844,309) and Hotta et al (6,023,096) in view of Otsuki et al (4,301,464).

10. Takigawa et al and Hotta et al disclose all above claimed subject matter however, Takigawa et al and Hotta et al do not disclose wherein a surface of the peripheral side face of the semiconductor element includes a micro crack, and the resin binder covering the peripheral side face of the semiconductor element reinforces the peripheral side face having the micro crack.

Otsuki et al discloses wherein a surface of the peripheral side face of the semiconductor element includes a micro crack, and the resin binder covering the peripheral side face of the semiconductor element reinforces the peripheral side face having the micro crack (column 1, lines 47-68 thru column 2, lines 1-6).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Takigawa et al and Hotta et al, with the teachings of Otsuki et al, for the purpose of bonding a tab to a semiconductor element in order to minimize the semiconductor element cracking when resin flows.

#### ***Response to Arguments***

11. Applicant's arguments with respect to claims 1-4, 6, 9 and 10 have been considered but are moot in view of the new ground(s) of rejection.

***Allowable Subject Matter***

12. Claims 11-20 are allowed over the prior art of record.

***Reasons for Allowance***

13.. The following is an examiner's statement of reasons for allowance: The prior art does not disclose nor fairly suggest a semiconductor device assembling method as provided in independent claim 11.

The first surface to which the semiconductor element is formed has been polished while the second surface is finished in order to remove a damaged layer which makes a very thin semiconductor element.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/  
Examiner, Art Unit 2813

/Carl Whitehead Jr./  
Supervisory Patent Examiner, Art Unit  
2813

mdh  
February 14, 2008